

CLAIMS

What is claimed is:

1           1.       A system using a current controlled charging circuit for charging columns  
2 of a liquid crystal display, said system comprising:

3               a liquid crystal display (LCD) having a matrix of liquid crystal pixels, said  
4 matrix comprising a plurality of columns and a plurality of rows, wherein an  
5 intersection of a row and a column defines a location of a pixel; and

6               at least one digital-to-analog converter (DAC) adapted to receive digital  
7 inputs representative of pixel gray scales, said at least one DAC having an output  
8 adapted for charging each of said plurality of columns to voltages representing  
9 said pixel gray scales, wherein the output comprises current source pulses having  
10 amplitudes and pulse-widths that charge each of said plurality of columns to said  
11 voltages.

1           2.       The system of claim 1, wherein a plurality of row switches selectively  
2 couples said matrix of pixels to said plurality of columns.

1           3.       The system of claim 2, wherein a plurality of column switches selectively  
2 couples the output of said at least one DAC to each of said plurality of columns.

1           4.       The system of claim 3, wherein column control logic controls said  
2 plurality of column switches and row control logic controls said plurality of row switches.

1           5.       The system of claim 4, further comprising an LCD pixel matrix address  
2 controller adapted for controlling said column and row control logic.

1           6.     The system of claim 5, further comprising a video frame to LCD pixel  
2     matrix address logic coupled to said LCD pixel matrix address controller, said video  
3     frame to LCD pixel matrix address logic adapted to receive video information and  
4     generate LCD pixel matrix addresses for said LCD pixel matrix address controller.

1           7.     The system of claim 1, further comprising a gray scale current pulse look-  
2     up table adapted for converting said pixel gray scales into the digital inputs received by  
3     said at least one DAC.

1           8.     The system of claim 7, further comprising a gray scale conversion logic  
2     coupled to said gray scale current pulse look-up table.

1           9.     The system of claim 8, wherein said gray scale conversion logic is adapted  
2     to receive video information and generate said pixel gray scales for said gray scale  
3     conversion logic.

1           10.    The system of claim 1, further comprising a pulse-width time control  
2     circuit for controlling the pulse-widths of said current source pulses.

1           11.    The system of claim 10, wherein said pulse-width time control circuit is  
2     coupled to a gray scale current pulse look-up table.

1           12.    The system of claim 10, wherein said pulse-width time control circuit is  
2     synchronized with a column clock.

1           13.    The system of claim 12, further comprising a phase-locked-loop (PLL)  
2   coupled between the column clock and a clock input to said pulse-width time control  
3   circuit, wherein said PLL is adapted to synchronize said clock input with said column  
4   clock.

1           14.    The system of claim 13, wherein said PLL generates said clock input to  
2   said pulse-width time control circuit.

1           15.    The system of claim 1, further comprising an analog-to-digital converter  
2   (ADC) for converting said voltages on said columns to digital voltage values.

1           16.    The system of claim 15, further comprising a digital comparator for  
2   comparing said voltages representing said pixel gray scales with said digital voltage  
3   values from said ADC.

1           17.    The system of claim 16, wherein comparisons of said voltages  
2   representing said pixel gray scales with said digital voltage values are used in determining  
3   compensation coefficients for each of said plurality of columns having different  
4   capacitance values.

1           18.    The system of claim 17, further comprising a memory for storing said  
2   compensation coefficients.

1           19.    The system of claim 1, wherein each of said plurality of columns has  
2   substantially the same capacitance.

1           20.    The system of claim 1, wherein each of said plurality of columns is  
2   compensated to have substantially the same capacitance.

1           21.    The system of claim 20, further comprising at least one capacitor  
2   connected to some ones of said plurality of columns such that each of said plurality of  
3   columns has substantially the same capacitance as another column.

1           22.    The system of claim 21, further comprising a column capacitance  
2   compensation circuit and at least one switch for coupling said at least one capacitor to  
3   said some ones of said plurality of columns.

1           23.    The system of claim 22, further comprising a column capacitance  
2   compensation memory coupled to said column capacitance compensation circuit, said  
3   column capacitance compensation memory storing connection setting for said at least one  
4   switch for coupling said at least one capacitor to said some ones of said plurality of  
5   columns.

1           24.    The system of claim 21, wherein said at least one capacitor is a plurality of  
2   capacitors having capacitance values in a binary progression.

1           25.    The system of claim 1, wherein said LCD is fabricated on a semiconductor  
2   integrated circuit.

1           26.    The system of claim 25, wherein said at least one DAC is fabricated on  
2   said semiconductor integrated circuit.

1           27.    The system of claim 3, wherein said plurality of column switches and said  
2 plurality of row switches are fabricated on a semiconductor integrated circuit.

1           28.    The system of claim 4, wherein said column control logic and said row  
2 control logic are fabricated on a semiconductor integrated circuit.

1           29.    The system of claim 5, wherein said LCD pixel matrix address controller  
2 is fabricated on a semiconductor integrated circuit.

1           30.    The system of claim 6, wherein said video frame to LCD pixel matrix  
2 address logic is fabricated on a semiconductor integrated circuit.

1           31.    The system of claim 7, wherein said gray scale current pulse look-up table  
2 is fabricated on a semiconductor integrated circuit.

1           32.    The system of claim 8, wherein said gray scale conversion logic is  
2 fabricated on a semiconductor integrated circuit.

1           33.    The system of claim 10, wherein said pulse-width time control circuit is  
2 fabricated on a semiconductor integrated circuit.

1           34.    The system of claim 11, wherein said gray scale current pulse look-up  
2 table is fabricated on a semiconductor integrated circuit.

1           35.    The system of claim 16, wherein said comparator and said ADC are  
2 fabricated on a semiconductor integrated circuit.

1           36.    The system of claim 22, wherein said column capacitance compensation  
2 circuit and said at least one switch are fabricated on a semiconductor integrated circuit.

1           37.    A current controlled charging circuit adapted for charging columns of a  
2 liquid crystal display having a matrix of liquid crystal pixels, said current controlled  
3 charging circuit comprising:

4                   at least one digital-to-analog converter (DAC) adapted to receive digital  
5 inputs representative of pixel gray scales, said at least one DAC having an output  
6 adapted for charging each of a plurality of columns of a liquid crystal display  
7 (LCD) to voltages representing said pixel gray scales, wherein the output  
8 comprises current source pulses having amplitudes and pulse-widths that charge  
9 each of said plurality of columns to said voltages.

1           38.    The current controlled charging circuit of claim 37, further comprising a  
2 gray scale current pulse look-up table adapted for converting said pixel gray scales into  
3 the digital inputs received by said at least one DAC.

1           39.    The current controlled charging circuit of claim 38, further comprising a  
2 gray scale conversion logic coupled to said gray scale current pulse look-up table.

1           40.    The current controlled charging circuit of claim 39, wherein said gray  
2 scale conversion logic is adapted to receive video information and generate said pixel  
3 gray scales for said gray scale conversion logic.

1           41.    The current controlled charging circuit of claim 37, further comprising a  
2   pulse-width time control circuit for controlling the pulse-widths of said current source  
3   pulses.

1           42.    The current controlled charging circuit of claim 41, wherein said pulse-  
2   width time control circuit is coupled to a gray scale current pulse look-up table.

1           43.    The current controlled charging circuit of claim 41, wherein said pulse-  
2   width time control circuit is synchronized with a column clock.

1           44.    The current controlled charging circuit of claim 43, further comprising a  
2   phase-locked-loop (PLL) coupled between the column clock and a clock input to said  
3   pulse-width time control circuit, wherein said PLL is adapted to synchronize said clock  
4   input with said column clock.

1           45.    The current controlled charging circuit of claim 44, wherein said PLL  
2   generates said clock input to said pulse-width time control circuit.

1           46.    The current controlled charging circuit of claim 37, further comprising a  
2   comparator circuit for comparing said voltages representing said pixel gray scales with  
3   said voltages from said ADC.

1           47.    The current controlled charging circuit of claim 46, wherein comparisons  
2   of said voltages representing said pixel gray scales with said voltage are used in  
3   determining compensation coefficients for each of said plurality of columns having  
4   different capacitance values.

1           48.    The current controlled charging circuit of claim 47, further comprising a  
2   memory for storing said compensation coefficients.

1           49.    A method using a current controlled charging circuit for charging columns  
2   of a liquid crystal display, said method comprising the steps of:

3                   providing a liquid crystal display (LCD) having a matrix of liquid crystal  
4           pixels, said matrix comprising a plurality of columns and a plurality of rows,  
5           wherein an intersection of a row and a column defines a location of a pixel; and  
6                   charging with a current controlled charging circuit each of said plurality of  
7           columns to voltages representing pixel gray scales.

1           50.    The method of claim 49, wherein the current controlled charging circuit is  
2   a current output digital-to-analog converter (DAC).

1           51.    The method of claim 49, further comprising the step of selectively  
2   coupling said matrix of pixels to said plurality of columns.

1           52.    The method of claim 49, wherein the step of charging is done with current  
2   pulses.

1           53.    The method of claim 52, further comprising the step of controlling  
2   amplitudes of said current pulses.

1           54.    The method of claim 52, further comprising the step of controlling pulse-  
2   widths of said current pulses.



1           55.    The method of claim 54, wherein the pulse-widths are determined with a  
2   gray scale current pulse look-up table.

1           56.    The method of claim 49, further comprising the step of measuring the  
2   voltages on said plurality of columns.

1           57.    The method of claim 56, further comprising the step of comparing the  
2   voltages representing the pixel gray scales with the voltages measured on said plurality of  
3   columns.

1           58.    The method of claim 57, further comprising the step of determining  
2   compensation coefficients from differences between the voltages representing the pixel  
3   gray scales and the voltages measured on said plurality of columns for each of said  
4   plurality of columns.

1           59.    The method of claim 58, further comprising the step of storing the  
2   compensation coefficients in a memory.

1           60.    The method of claim 49, further comprising the step of adding  
2   compensating capacitance to said plurality of columns such that each of said plurality of  
3   columns has substantially the same capacitance as the others.

1           61.    The system of claim 1, further comprising a circuit for setting said  
2   plurality of columns to a desired voltage before charging said plurality of columns to said  
3   voltages.

1           62.    The system of claim 61, wherein the desired voltage is substantially zero.

1           63.    The system of claim 1, further comprising a circuit for discharging said  
2 plurality of columns before charging said plurality of columns to said voltages.

1           64.    The system of claim 1, further comprising a comparison circuit for  
2 comparing said voltages representing said pixel gray scales with said voltages on said  
3 columns, said comparison circuit output being used in determining compensation  
4 coefficients for each of said plurality of columns having different capacitance values.

1           65.    The system of claim 20, wherein each of said plurality of columns is  
2 compensated with a fuse link connected plurality of capacitors.

1           66.    The method of claim 60, wherein the step of adding compensating  
2 capacitance to said plurality of columns comprises the steps of blowing fuse links  
3 connected to a plurality of compensation capacitors.